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Wafer Bonding and the Integration of MEMS into 3D Devices

There is a very high level of interest and investment in the area of 3DIC (Three Dimensional Integrated Circuit) by all of the major IC designers, manufacturers, and product designers. This interest is driven by the potential performance improvements in terms of increased speed, lower power consumption, reduced package size and the ability to mix heterogeneous processes such as memory and processor. These potential benefits of 3D integration are not limited to the IC domain; they are also of interest to MEMS (Micro Electro Mechanical Systems). The concept of combining the MEMS sensor with A/D conversion along with memory and processing in a single package is very powerful. Customized MEMS devices can be integrated with standardized modules, which significantly reduce the design complexity and especially the time-to-market. This presentation will review with emphasis on the design considerations: 1) The current 3D integration flows applicable to MEMs along with their strengths and weaknesses. 2) The wafer to wafer, chip to wafer, and chip to chip process flows. 3.) The major alignment techniques. 4.) The major bonding techniques. (These techniques will apply to wafer to wafer, chip to wafer and chip to chip. 5.) The process of selecting a bonding process. 6.) The effect of the bonding process that is selected on the design rules and chip layout. 7.) Some of the common pitfalls and 8.) Known product applications.